ESE 382 Digital Design Using VHDL and PLDs

K. Short, Spring 07, *revised January 11, 2007 11:53 am*

Lecture: Tu. and Th., 2:20 to 3:40 in room 102 Light Engineering building.
Office Hours: Tu. and Th. 8:30 to 10:30 am in room 229 Light Engineering building.

Modern design methodologies allow complex digital systems to be rapidly designed, veri fied, and implemented using a hardware description language and programmable ICs. The key elements in these methodologies are:

1. Use of a hardware description language (HDL) to describe (model) the system.
2. Use of a simulator to functionally simulate the HDL description.
3. Use of electronic design automation (EDA) software tools to synthesize a gate-level representation from the HDL description.
4. Use of a place-and-route EDA tool to map the synthesized logic to a programmable logic device (PLD).
5. Use of a simulator to simulate the timing of the synthesized logic mapped to the target PLD.
6. Use of a high logic capacity PLD for immediate implementation of the system.

Expertise in design using an HDL is a critical requirement for digital designers. The most popular hardware description language is VHDL (Very high speed integrated circuit Hardware Description Language). The designer writes a description of the desired system in VHDL. The designer also writes an associated testbench in VHDL. During simulation, the testbench provides stimulus inputs to the design description and verifies its outputs.

Using the testbench, the VHDL design description is simulated to verify that the system, as described, meets its functional specification. Then, a VHDL synthesizer and a place and route tool are used to create two files. One file is a VHDL timing model of the synthesized logic fitted to the target PLD. This model is simulated to verify that the design will meet the system's timing requirements. The other file is a configuration file used to program the target PLD.

Course Objectives

The primary course objectives are for you to:

1. Strengthen and extend your understanding of the theory and fundamentals of digital system design.
2. Learn the hardware description language VHDL and become proficient in a design methodology that uses VHDL to create and verify systems that are implemented in PLDs.
3. Learn the architecture and operation of various PLDs: SPLDs, CPLDs, and FPGAs.

Prerequisite
The prerequisite for this course is ESE 218 Digital System Design.

Course Material:

1. Draft text (provided by the instructor). The first volume of this draft (Chapters 1 through 7) will be distributed after the first class meeting (January 23rd) in the DSRP Laboratory (room 228 Light Engineering building).
2. Data sheets and other written material, including lecture notes and laboratory assignments (provided on Blackboard).

Digital System Rapid Prototyping (DSRP) Laboratory
Each week you will implement a design during your assigned three hour laboratory session in the DSRP Laboratory (room 228 Light Engineering building). Prior to each of your laboratory sessions, you will write and simulate your VHDL code for the design. Simulations can be performed in the ECE CAD Laboratory (room 281 Light Engineering building).

In the DSRP Laboratory, you will use a synthesizer and place-and-route tool to produce a VHDL timing model of the design and a configuration file for programming a PLD. Using the timing model you will perform a timing simulation of the design. After the timing simulation, you will program and test a PLD. Laboratory sessions start the week beginning January 28th.

Grades
Course grades are based on:

Exams (2) 46%
Quizzes (5) 20%
Laboratories (once a week, three hours) 34%

The tentative exam dates are:

Exam 1 - March 1st (Thursday)
Exam 2 - April 19th (Thursday)

Your lowest lab, excluding the last two labs, will be dropped from your lab average. The dates of the quizzes will not be announced. Your lowest quiz will be dropped from your quiz average. ***No make-up exams, quizzes, or laboratories will be provided.***

Tentative Lecture Schedule
The lectures are presented based on the assumption that students have completed the assigned reading prior to the lecture. A lecture handout will be available on Blackboard for each lecture the prior week to the lecture. It is recommended that you print this handout and bring it to lecture. The intention is to cover one chapter of the text each week. A more detailed schedule will be

provided on Blackboard.

Blackboard
You can access class information on-line at: http://blackboard.sunysb.edu If you used Blackboard during the Fall semester, your login information (Username and Password) has not changed. If you have never used Stony Brook's Blackboard system, your initial password is your SOLAR ID# and your username is the same as your Stony Brook (sparky) username, which is generally your first initial and the first 7 letters of your last name. For help or more information see:

For help or more information see: http://www.sinc.sunysb.edu/helpdesk/docs/blackboard/bbstudent.php

For problems logging in, go to the helpdesk in the Main Library SINC Site or the Union SINC Site, you can also call: 631-632-9602 or e-mail: helpme@ic.sunysb.edu
The following statement is included at the request of the Provost.

If you have a physical, psychological, medical or learning disability that may impact on your ability to carry out assigned course work, you are urged to contact the staff in the Disabled Student Services office (DSS), Room 133 Humanities, 632-6748/TDD. DSS will review your concerns and determine, with you, what accommodations are necessary and appropriate.